

# Hi-performance Regulator IC Series for PCs

## Nch FET Ultra LDOs

## for Desktop PCs Chipsets with Power Good



BD3540NUV, BD3541NUV

No.09030EBT04

### ●Description

The BD3540NUV, BD3541NUV low-voltage output linear 1ch series chipset regulator IC operates from a very low input supply, and offers ideal performance in low input voltage to low output voltage applications. It incorporates a built-in N-MOSFET power transistor to minimize the input-to-output voltage differential to the ON resistance ( $R_{ON}=200m\Omega\sim 400m\Omega$ ) level. By lowering the dropout voltage in this way, the regulator realizes high current output ( $I_{omax}=0.5A\sim 1.0A$ ) with reduced conversion loss, and thereby obviates the switching regulator and its power transistor, choke coil, and rectifier diode. Thus, the BD3540NUV, BD3541NUV are designed to enable significant package profile downsizing and cost reduction. An external resistor allows the entire range of output voltage configurations between 0.65 and 2.7V, while the NRCS (soft start) function enables a controlled output voltage ramp-up, which can be programmed to whatever power supply sequence is required.

### ●Features

- 1) High-precision voltage regulator( $0.65V\pm 1\%$ )
- 2) Built-in VCC undervoltage lockout circuit
- 3) NRCS (soft start) function reduces the magnitude of in-rush current
- 4) Internal Nch MOSFET driver offers low ON resistance
- 5) Built-in current limit circuit
- 6) Built-in thermal shutdown (TSD) circuit
- 7) Variable output
- 8) Small package VSON010V3030 :  $3.0\times 3.0\times 1.0(mm)$
- 9) Tracking function

### ●Applications

Notebook computers, Desktop computers, LCD-TV, DVD, Digital appliances

### ●Line-up

It is available to select power supply voltage and maximum output voltage.

| Maximum Output Voltage | Package      | Vcc=5V    |
|------------------------|--------------|-----------|
| 0.5A                   | VSON010V3030 | BD3540NUV |
| 1.0A                   |              | BD3541NUV |

●Absolute maximum ratings

◎BD3540NUV, BD3541NUV

| Parameter                   | Symbol      | Limit              |           | Unit |
|-----------------------------|-------------|--------------------|-----------|------|
|                             |             | BD3540NUV          | BD3541NUV |      |
| Input Voltage 1             | $V_{CC}$    | +6.0 <sup>*1</sup> |           | V    |
| Input Voltage 2             | $V_{IN}$    | +6.0 <sup>*1</sup> |           | V    |
| Enable Input Voltage        | $V_{en}$    | -0.3~+6.0          |           | V    |
| PGOOD Input Voltage         | $V_{PGOOD}$ | +6.0 <sup>*1</sup> |           | V    |
| Power Dissipation 1         | $P_{d1}$    | 0.70 <sup>*2</sup> |           | W    |
| Power Dissipation 2         | $P_{d2}$    | 1.27 <sup>*2</sup> |           | W    |
| Power Dissipation 3         | $P_{d3}$    | 3.03 <sup>*2</sup> |           | W    |
| Operating Temperature Range | $T_{opr}$   | -10~+100           |           | °C   |
| Storage Temperature Range   | $T_{stg}$   | -55~+150           |           | °C   |
| Junction Temperature        | $T_{jmax}$  | +150               |           | °C   |

\*1 Should not exceed  $P_d$ .

\*2 Reduced by 5.6mW/°C for each increase in  $T_a \geq 25^\circ\text{C}$  (when mounted on a 74.2mm × 74.2mm × 1.6mm glass-epoxy board, 1-layer)  
On less than 0.2% (percentage occupied by copper foil).

\*3 Reduced by 10.1mW/°C for each increase in  $T_a \geq 25^\circ\text{C}$  (when mounted on a 74.2mm × 74.2mm × 1.6mm glass-epoxy board, 1-layer)  
On less than 7.0% (percentage occupied by copper foil).

\*4 Reduced by 24.2mW/°C for each increase in  $T_a \geq 25^\circ\text{C}$  (when mounted on a 74.2mm × 74.2mm × 1.6mm glass-epoxy board, 1-layer)  
On less than 65.0% (percentage occupied by copper foil).

●Operating Voltage( $T_a=25^\circ\text{C}$ )

◎BD3540NUV, BD3541NUV

| Parameter                    | Symbol      | Min.     | Max.                       |           | Unit |
|------------------------------|-------------|----------|----------------------------|-----------|------|
| Input Voltage 1              | $V_{CC}$    | 3.0      | 5.5                        |           | V    |
| Input Voltage 2              | $V_{IN}$    | 0.95     | $V_{CC}-1$ <sup>*1*5</sup> |           | V    |
| Output Voltage               | $I_O$       | -        | BD3540NUV                  | BD3541NUV | A    |
|                              |             |          | 0.5                        | 1.0       |      |
| PGOOD Input Voltage          | $V_{PGOOD}$ | -0.3     | 5.5                        |           | V    |
| Output Voltage Setting Range | $V_O$       | $V_{FB}$ | 2.7                        |           | V    |
| Enable Input Voltage         | $V_{en}$    | 0        | 5.5                        |           | V    |

\*5  $V_{CC}$  and  $V_{IN}$  do not have to be implemented in the order listed.

\*This product is not designed for use in radioactive environments.

●Attention : About this document

The official specification of this product (BD354XNUV) is the Japanese version.

This translation is intended only as a reference to understand the official version.

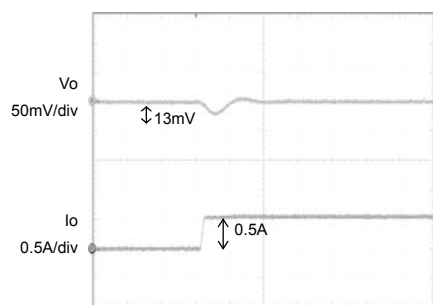
If there are any differences between the Japanese and this translated version, the official Japanese version takes priority.

## ●Electrical Characteristics

(Unless otherwise specified, Ta=25°C, VCC=5V, Ven=3V, VIN=1.7V, R1=3.9KΩ, R2=3.3KΩ)

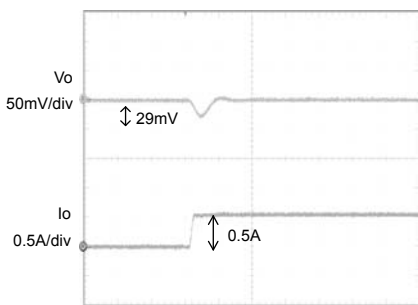
| Parameter                                   | Symbol              | Limit     |          |            | Unit | Condition  |
|---|---------------------|-----------|----------|------------|------|--|
|   |                     | Min.      | Typ.     | Max.       |      |  |
| Bias Current                                | ICC                 | -         | 0.7      | 1.0        | mA   |  |
| VCC Shutdown Mode Current                   | IST                 | -         | 0        | 10         | μA   | Ven=0V   |
| Output Voltage                              | VO                  | -         | 1.200    | -          | V    |  |
| Output Voltage Temperature Coefficient      | Tcvo                | -         | 0.01     | -          | %/°C |  |
| Feedback Voltage 1                          | VFB1                | 0.643     | 0.650    | 0.657      | V    |  |
| Feedback Voltage 2                          | VFB2                | 0.637     | 0.650    | 0.663      | V    | Tj=-10 to 100°C  |
| Load Regulation                             | Reg.L               | -         | 0.5      | 10         | mV   | (BD3540NUV Io=0A to 0.5A)<br>(BD3541NUV Io=0A to 1.0A) |
| Line Regulation 1                           | Reg.I1              | -         | 0.1      | 0.5        | %/V  | VCC=3.0V to 5.5V                                       |
| Line Regulation 2                           | Reg.I2              | -         | 0.1      | 0.5        | %/V  | VIN=1.5V to 3.3V                                       |
| Standby Discharge Current                   | I <sub>den</sub>    | 1         | -        | -          | mA   | Ven=0V, Vo=1V  |
| [ENABLE]                                    |                     |           |          |            |      |  |
| Enable Pin Input Voltage High               | Enhi                | 2         | -        | -          | V    |  |
| Enable Pin Input Voltage Low                | Enlow               | 0         | -        | VCC × 0.15 | V    |  |
| Enable Input Bias Current                   | I <sub>en</sub>     | -         | 7        | 10         | μA   | Ven=3V   |
| [NRCS]                                      |                     |           |          |            |      |  |
| NRCS Charge Current                         | I <sub>nr</sub>     | 14        | 20       | 26         | μA   | Vnr=0.5V   |
| NRCS Standby Voltage                        | VSTB                | -         | 0        | 50         | mV   | Ven=0V   |
| [UVLO]                                      |                     |           |          |            |      |  |
| VCC Undervoltage Lockout Threshold Voltage  | V <sub>ccUVLO</sub> | 2.3       | 2.5      | 2.7        | V    | V <sub>cc</sub> :Sweep-up                              |
| VCC Undervoltage Lockout Hysteresis Voltage | V <sub>chys</sub>   | 50        | 100      | 150        | mV   | V <sub>cc</sub> :Sweep-down                            |
| [PGOOD]                                     |                     |           |          |            |      |  |
| Low-side Threshold Voltage                  | V <sub>THPGL</sub>  | VO × 0.87 | VO × 0.9 | VO × 0.93  | V    |  |
| High-side Threshold Voltage                 | V <sub>THPHG</sub>  | VO × 1.07 | VO × 1.1 | VO × 1.13  | V    |  |
| PGDLY charge current                        | I <sub>PGDLY</sub>  | 1.4       | 2.0      | 2.6        | μA   |  |
| Ron   | R <sub>PG</sub>     | 30        | 75       | 150        | Ω    |  |
| [AMP]                                       |                     |           |          |            |      |  |
| Minimum dropout voltage                     | BD3540NUV           | dVo       | -        | 200        | 300  | mV<br>Io=0.5A, VIN=1.2V,<br>Ta=-10 to 100°C            |
|   | BD3541NUV           | dvo       | -        | 200        | 300  | mV<br>Io=1.0A, VIN=1.2V,<br>Ta=-10 to 100°C            |

## ●Reference Data(BD3540NUV)



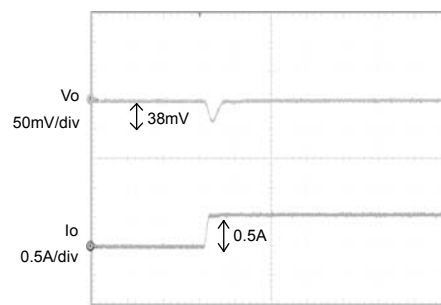
Io=0A→1A/μsec t(10μsec/div)

Fig.1 Transient Response  
(0→0.5A)  
Co=100μF, Cfb=1000pF



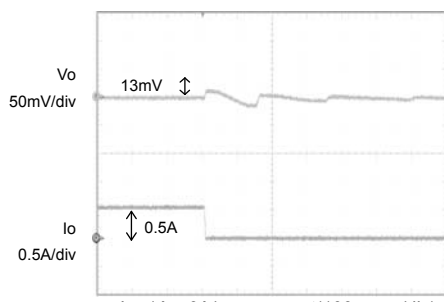
Io=0A→1A/μsec t(10μsec/div)

Fig.2 Transient Response  
(0→0.5A)  
Co=47μF, Cfb=1000pF



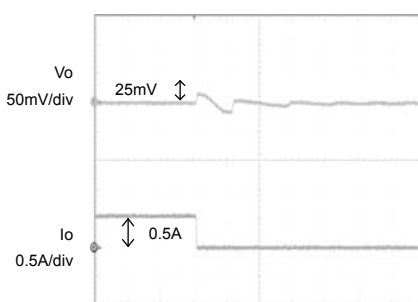
Io=0A→1A/μsec t(10μsec/div)

Fig.3 Transient Response  
(0→0.5A)  
Co=22μF, Cfb=1000pF



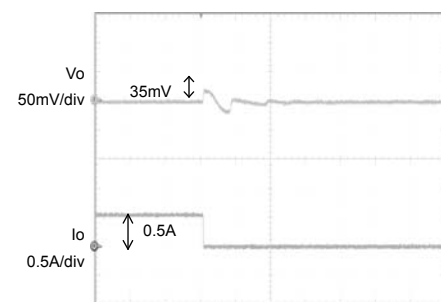
Io=1A→0A/μsec t(100μsec/div)

Fig.4 Transient Response  
(0.5→0A)  
Co=100μF, Cfb=1000pF



Io=1A→0A/μsec t(100μsec/div)

Fig.5 Transient Response  
(0.5→0A)  
Co=47μF, Cfb=1000pF



Io=1A→0A/μsec t(100μsec/div)

Fig.6 Transient Response  
(0.5→0A)  
Co=22μF, Cfb=1000pF

## ●Reference Data(BD3541NUV)

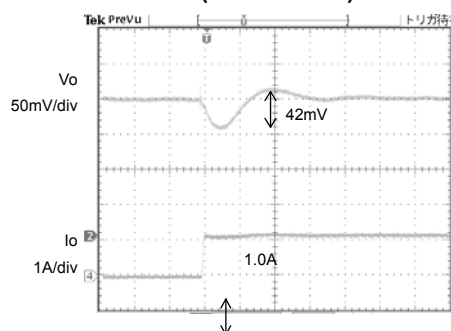


Fig.7 Transient Response  
(0→1.0A)  
Co=100μF, Cfb=1000pF

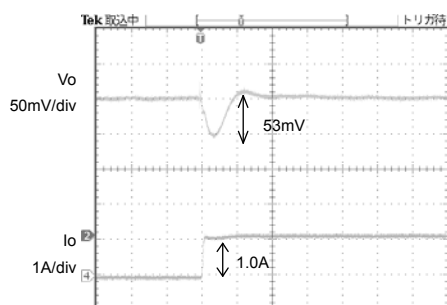


Fig.8 Transient Response  
(0→1.0A)  
Co=47μF, Cfb=1000pF

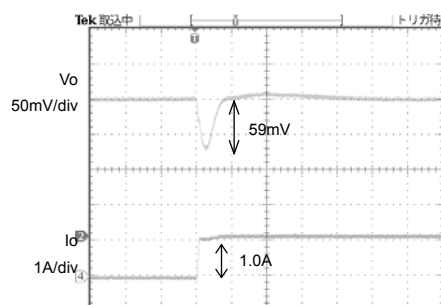


Fig.9 Transient Response  
(0→1.0A)  
Co=22μF, Cfb=1000pF

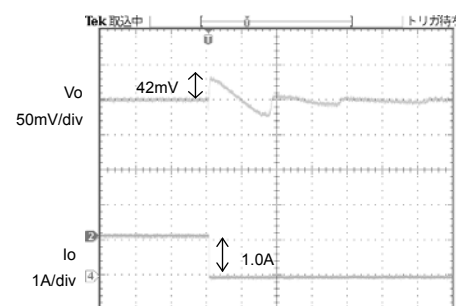


Fig.10 Transient Response  
(1.0→0A)  
Co=100μF, Cfb=1000pF

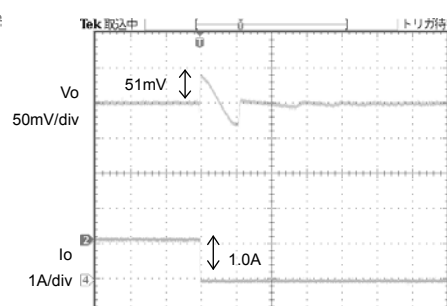


Fig.11 Transient Response  
(1.0→0A)  
Co=47μF, Cfb=1000pF

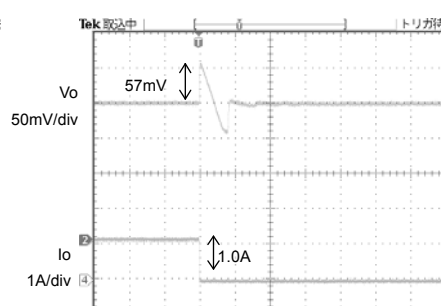


Fig.12 Transient Response  
(1.0→0A)  
Co=22μF, Cfb=1000pF

●Reference Data(BD3540NUV)

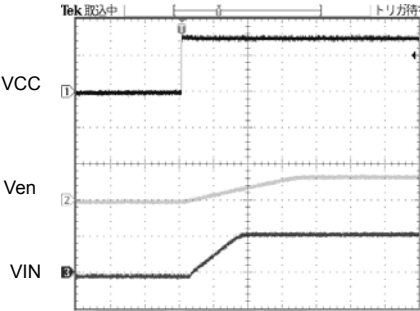


Fig.19 Waveform at output start

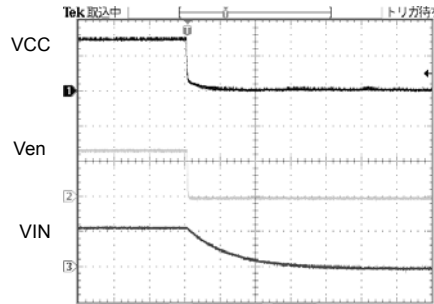


Fig.20 Waveform at output OFF

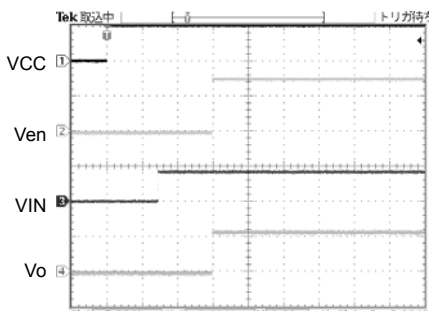


Fig.21 Input sequence

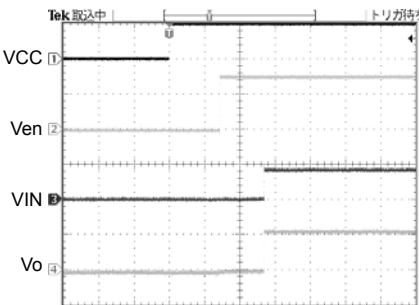


Fig.22 Input sequence

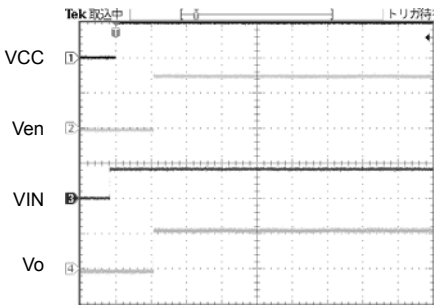


Fig.23 Input sequence

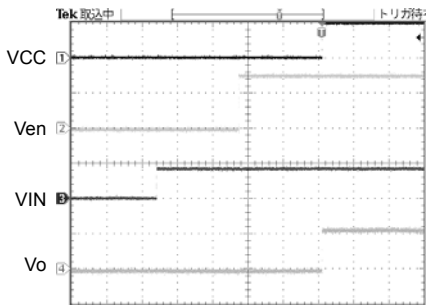


Fig.24 Input sequence

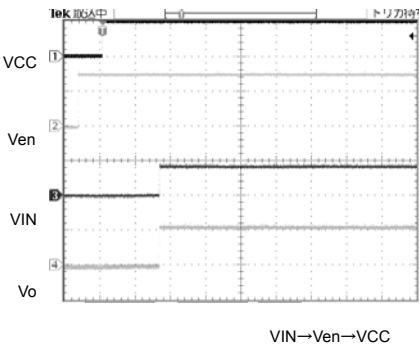


Fig.25 Input sequence

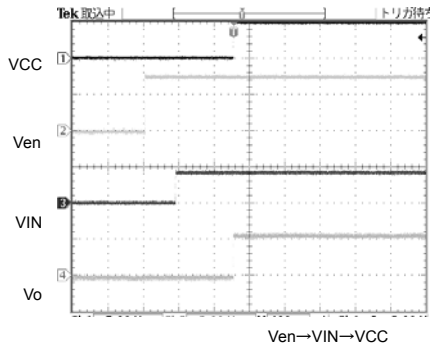


Fig.26 Input sequence

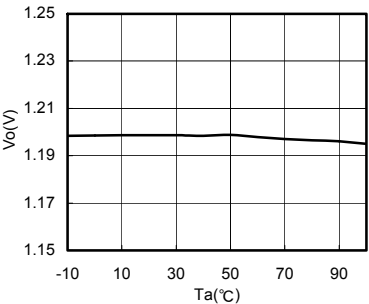


Fig.27 Ta-Vo (Io=0mA)

## ●Reference Data(BD3540NUV)

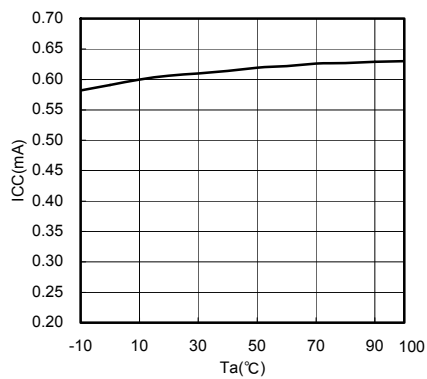


Fig.28 Ta-ICC

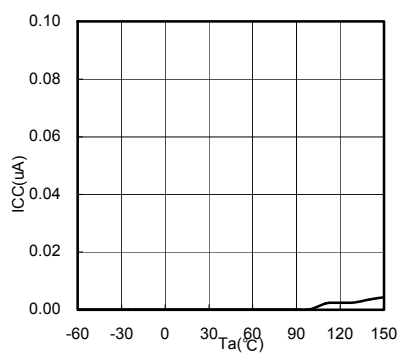


Fig.29 Ta-ISTB

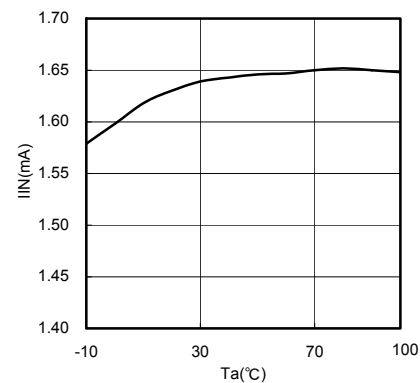


Fig.30 Ta-IIN

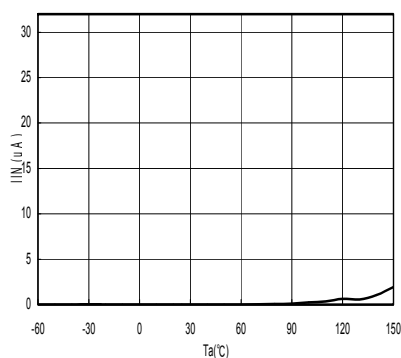


Fig.31 Ta-IINSTB

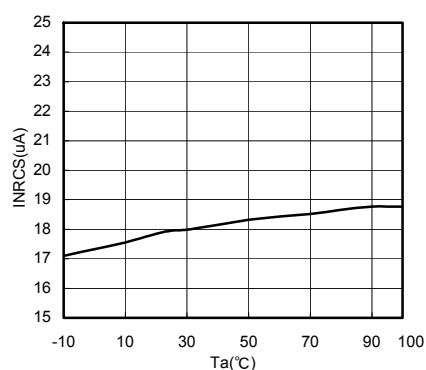


Fig.32 Ta-INRCS

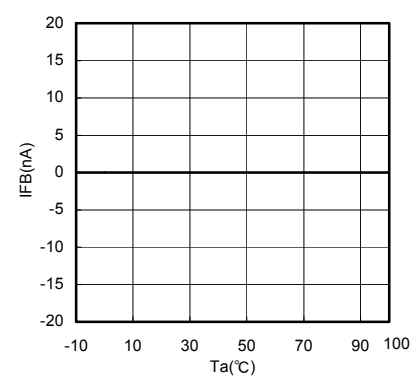


Fig.33 Ta-IFB

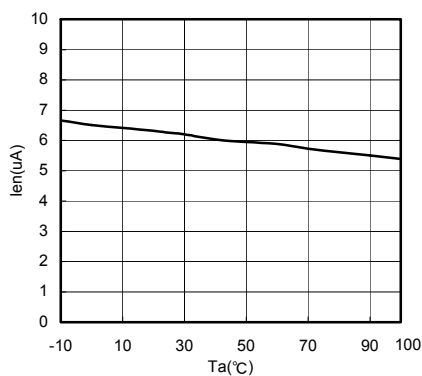


Fig.34 Ta-Ien

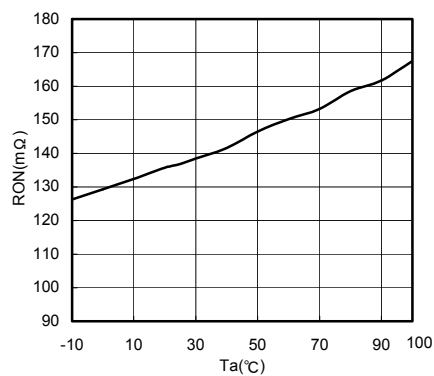
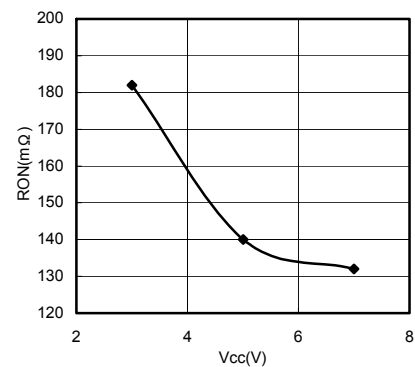
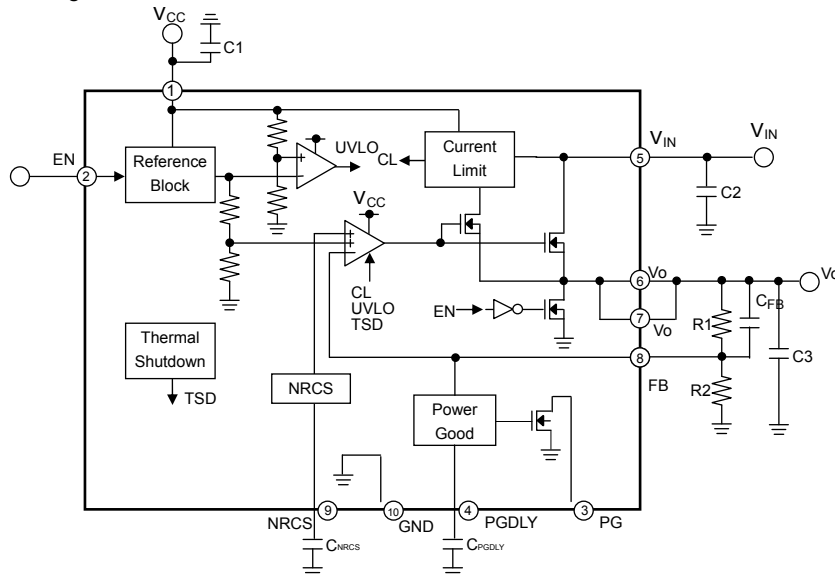
Fig.35 Ta-RON  
(VCC=5V/Vo=1.2V)

Fig.36 VCC-RON

## ●Block Diagram

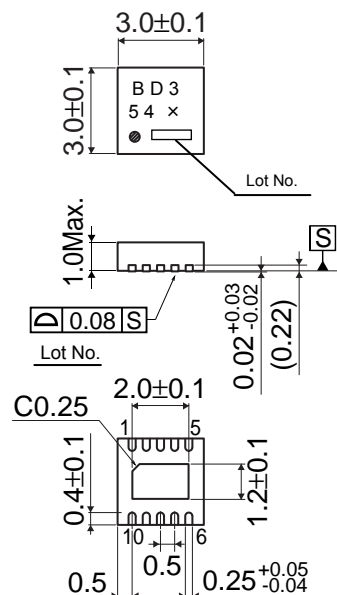


## ●Pin Function Table

| PIN No. | PIN name | PIN Function   |
|---------|----------|--|
| 1       | VCC      | Power supply pin   |
| 2       | EN       | Enable input pin   |
| 3       | PG       | Power Good pin   |
| 4       | PGDLY    | Power Good Delay capacitor connection pin                  |
| 5       | VIN      | Input voltage pin  |
| 6       | VO       | Output voltage pin   |
| 7       | VO       | Output voltage pin   |
| 8       | FB       | Reference voltage feedback pin                             |
| 9       | NRCS     | In-rush current protection (NRCS) capacitor connection pin |
| 10      | GND      | Ground pin   |

## ●Pin Layout

©VSON010V3030



(Unit : mm)

## ● Operation of Each Block

### • AMP

This is an error amp that compares the reference voltage (0.65V) with  $V_o$  to drive the output Nch FET ( $R_{on}=100m\Omega \sim 400m\Omega$ ). Frequency optimization helps to realize rapid transient response, and to support the use of ceramic capacitors on the output. AMP input voltage ranges from GND to 2.7V, while the AMP output ranges from GND to VCC. When EN is OFF, or when UVLO is active, output goes LOW and the output of the NchFET switches OFF.

### • EN

The EN block controls the regulator's ON/OFF state via the EN logic input pin. In the OFF position, circuit voltage is maintained at  $0\mu A$ , thus minimizing current consumption at standby. The FET is switched ON to enable discharge of the NRCS pin  $V_o$ , thereby draining the excess charge and preventing the IC on the load side from malfunctioning. Since no electrical connection is required (e.g., between the VCC pin and the ESD prevention Diode), module operation is independent of the input sequence.

### • UVLO

To prevent malfunctions that can occur during a momentary decrease in VCC, the UVLO circuit switches the output OFF, and (like the EN block) discharges NRCS and  $V_o$ . Once the UVLO threshold voltage (TYP2.5V) is reached, the power-on reset is triggered and output continues.

### • CURRENT LIMIT

When output is ON, the current limit function monitors the internal IC output current against the parameter value (2.0A or more:BD3540NUV). When current exceeds this level, the current limit module lowers the output current to protect the load IC. When the overcurrent state is eliminated, output voltage is restored to the parameter value.

### • NRCS (Non Rush Current on Start-up)

The soft start function enabled by connecting an external capacitor between the NRCS pin and ground. Output ramp-up can be set for any period up to the time the NRCS pin reaches VFB (0.65V). During startup, the NRCS pin serves as a  $20\mu A$  (TYP) constant current source to charge the external capacitor. Output start time is calculated via formula (1) below.

$$t = C \frac{0.65V}{20\mu A} \quad \cdot \cdot \cdot (1)$$

Tracking sequence is available by connecting the output voltage of external power supply instead of external capacitor. And then, ratio-metric sequence is also available by changing the resistor division ratio of external power supply output voltage. (See the next page)

### • TSD (Thermal Shut down)

The shutdown (TSD) circuit automatically switches output OFF when the chip temperature gets too high, thus serving to protect the IC against "thermal runaway" and heat damage. Because the TSD circuit is provided to shut down the IC in the presence of extreme heat, in order to avoid potential problems with the TSD, it is crucial that the  $T_j$  (max) parameter not be exceeded in the thermal design.

### • VIN

The VIN line acts as the major current supply line, and is connected to the output NchFET drain. Since no electrical connection (such as between the VCC pin and the ESD protection Diode) is necessary, VIN operates independent of the input sequence. However, since an output NchFET body Diode exists between VIN and  $V_o$ , a VIN- $V_o$  electric (Diode) connection is present. Note, therefore, that when output is switched ON or OFF, reverse current may flow to VIN from  $V_o$ .

### • PGOOD

It outputs the output voltage ( $V_o$ ). PGOOD pin (open drain) is used to pull up the  $100k\Omega$  resistor. PGOOD will be judged HIGH between the FB voltage 0.585V(TYP) to 0.715V(TYP), and will be judged LOW if the voltage is out of range.

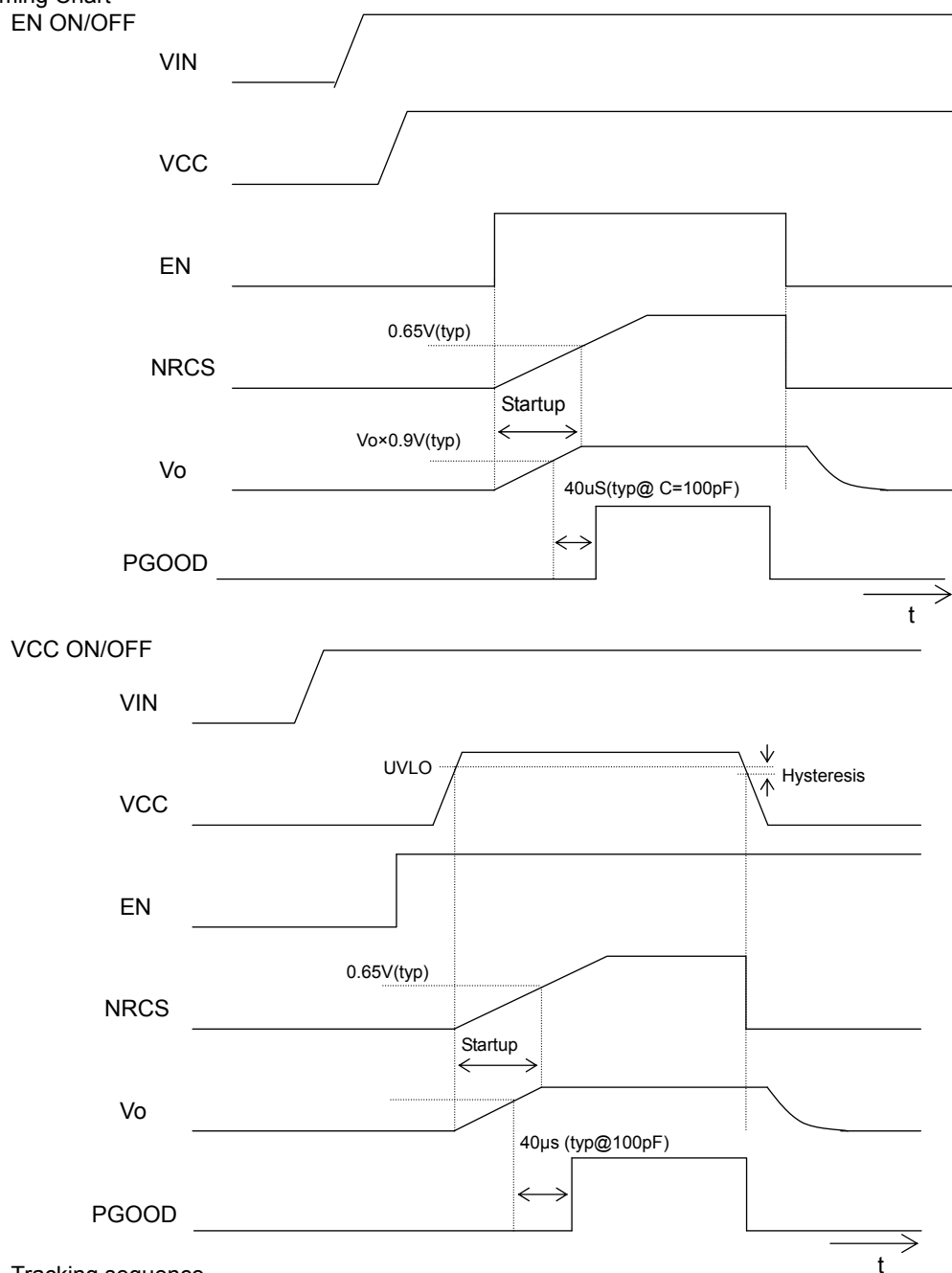
### • PGDLY

It is available to set PGOOD output delay. PGDLY pin should be connected to  $100pF$  capacitor. PGOOD delay time is determined by the following formula.

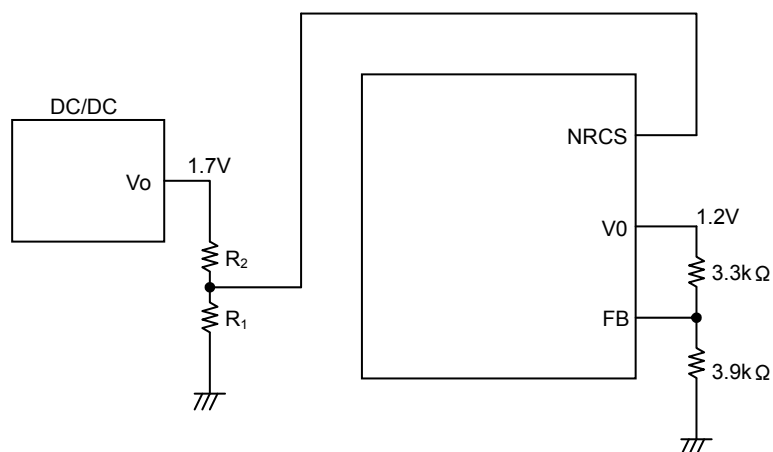
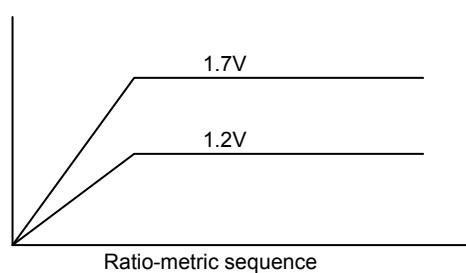
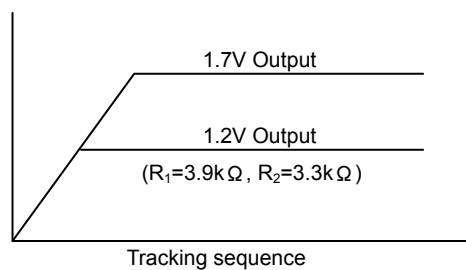
$$t_{pgdly} = \frac{C(pF) \times 0.75}{I_{pgdly} (\mu A)} \quad (\mu sec)$$



● Timing Chart  
EN ON/OFF

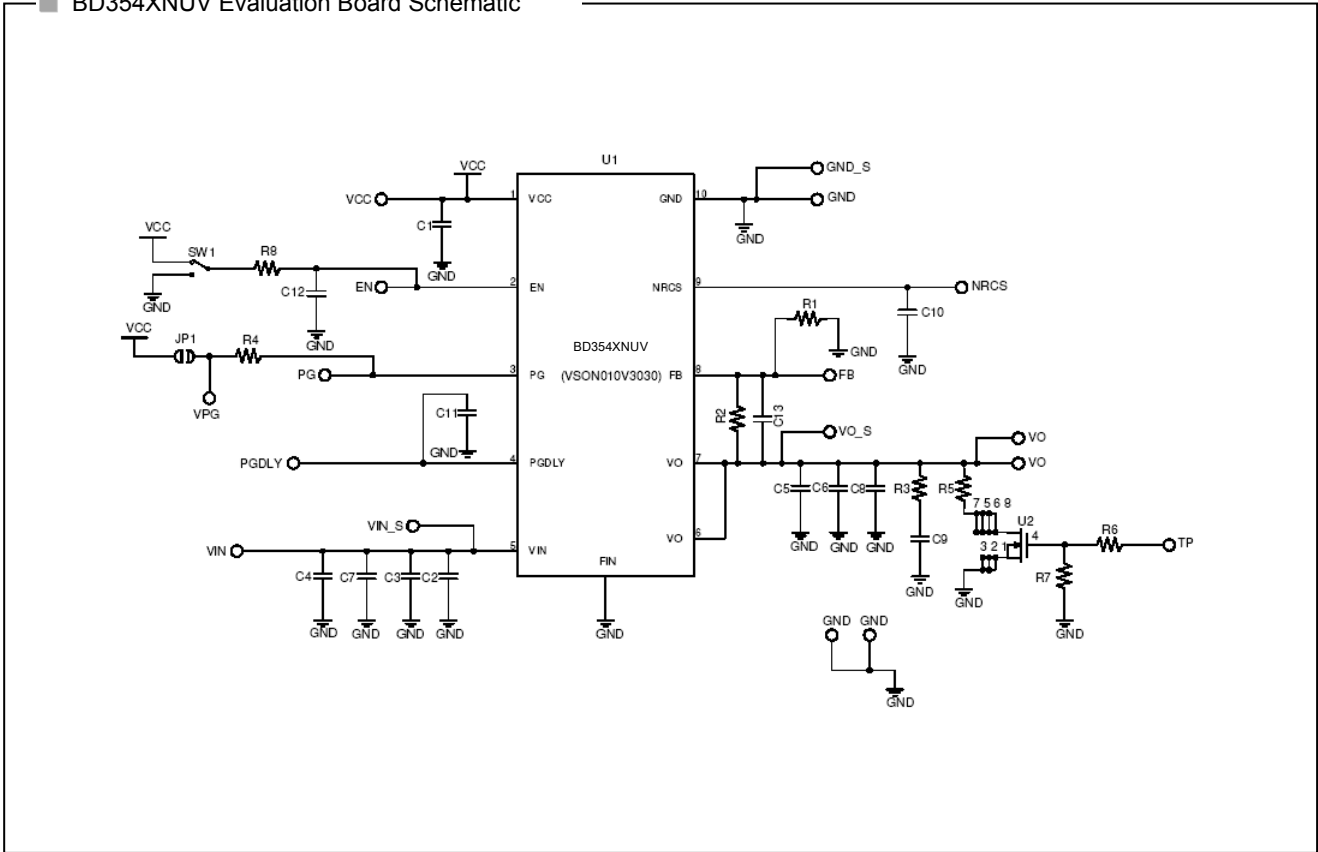


Tracking sequence



●Evaluation Board

■ BD354XNUV Evaluation Board Schematic

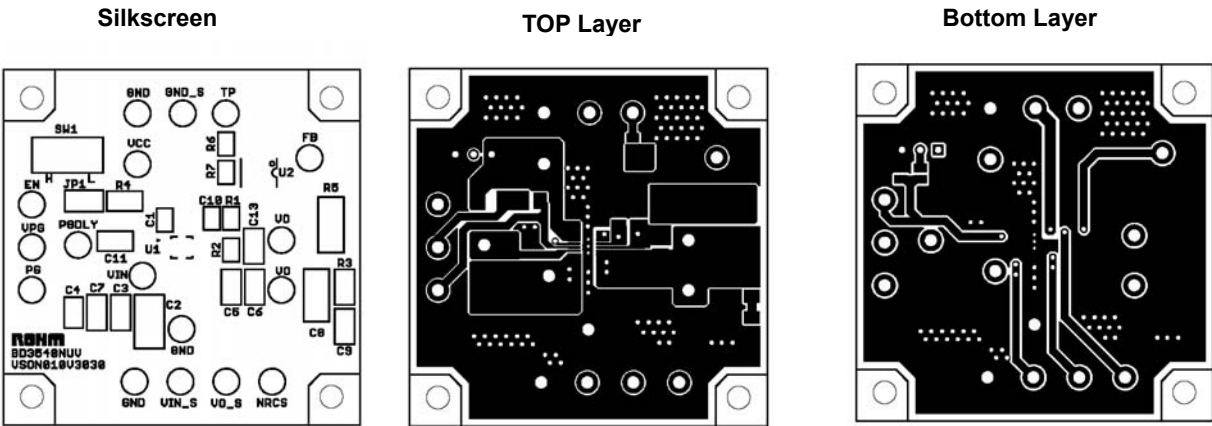


■ BD354XNUV Evaluation Board Standard Component List

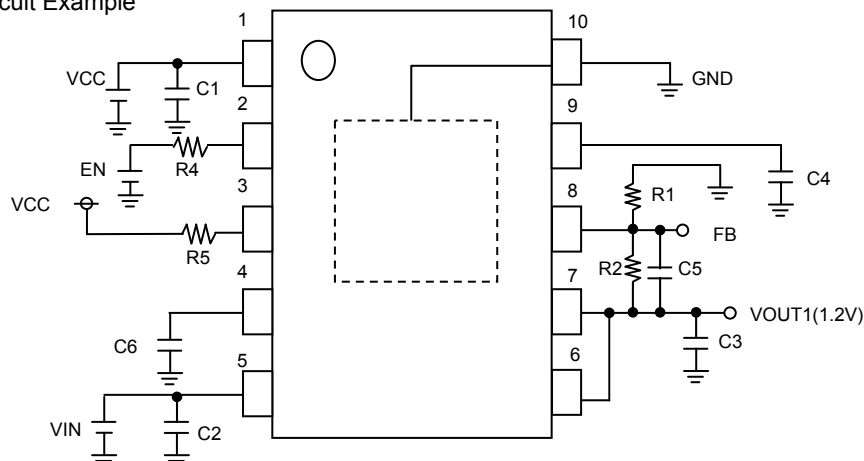
| Component | Rating | Manufacturer | Product Name    |
|-----------|--------|--------------|-----------------|
| U1        | -      | ROHM         | BD354XNUV       |
| C1        | 1uF    | MURATA       | GRM188B11A105KD |
| C10       | 0.01uF | MURATA       | GRM188B11H103KD |
| R8        | 0Ω     | -            | Jumper          |
| C5        | 22uF   | KYOCERA      | CM32X5R226M10A  |

| Component | Rating | Manufacturer | Product Name    |
|-----------|--------|--------------|-----------------|
| C2        | 22uF   | KYOCERA      | CM32X5R226M10A  |
| C13       | 1000pF | MURATA       | GRM188B11H102KD |
| R1        | 3.9kΩ  | ROHM         | MCR03EZPF3301   |
| R2        | 3.3kΩ  | ROHM         | MCR03EZPF3901   |
| R4        | 100kΩ  | ROHM         | MCR03EZPF       |

■ BD354XNUV Evaluation Board Layout  
(2nd layer and 3rd layer are GND Line.)

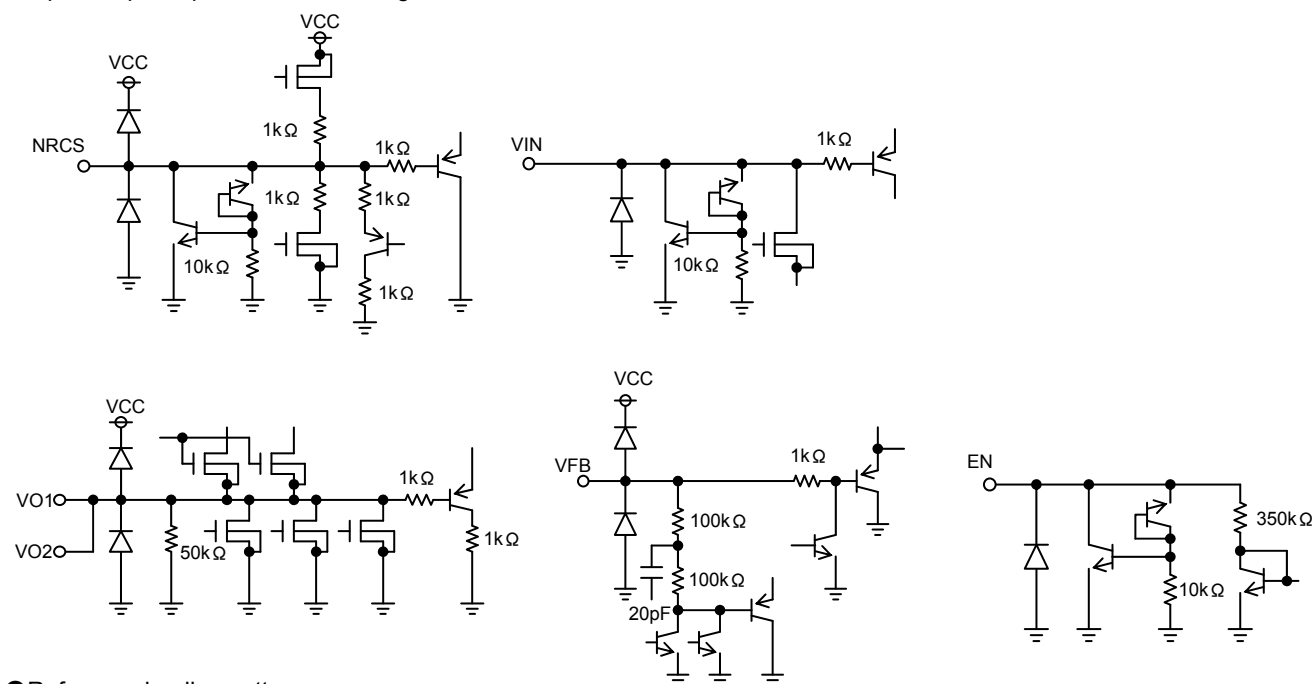


## ●Recommended Circuit Example

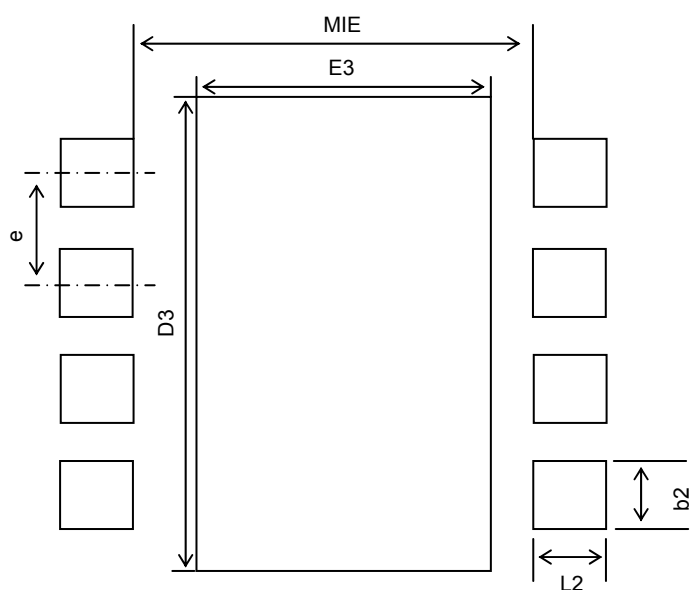


| Component | Recommended Value                                       | Programming Notes and Precautions   |
|-----------|---|---|
| R1/R2     | 3.9k/3.3k   | IC output voltage can be set with a configuration formula using the values for the internal reference output voltage ( $V_{FB}$ ) and the output voltage resistors (R1, R2). Select resistance values that will avoid the impact of the VREF current ( $\pm 100\text{nA}$ ). The recommended total resistance value is $10\text{k}\Omega$ .   |
| C3        | $22\mu\text{F}$   | To assure output voltage stability, please be certain the VOUT1 pins and the GND pins are connected. Output capacitors play a role in loop gain phase compensation and in mitigating output fluctuation during rapid changes in load level. Insufficient capacitance may cause oscillation, while high equivalent series resistance (ESR) will exacerbate output voltage fluctuation under rapid load change conditions. While a $22\mu\text{F}$ ceramic capacitor is recommended, actual stability is highly dependent on temperature and load conditions. Also, note that connecting different types of capacitors in series may result in insufficient total phase compensation, thus causing oscillation. In light of this information, please confirm operation across a variety of temperature and load conditions. |
| C1        | $1\mu\text{F}$  | Input capacitors reduce the output impedance of the voltage supply source connected to the (VCC) input pins. If the impedance of this power supply were to increase, input voltage (VCC) could become unstable, leading to oscillation or lowered ripple rejection function. While a low-ESR $1\mu\text{F}$ capacitor with minimal susceptibility to temperature is recommended, stability is highly dependent on the input power supply characteristics and the substrate wiring pattern. In light of this information, please confirm operation across a variety of temperature and load conditions.  |
| C2        | $22\mu\text{F}$   | Input capacitors reduce the output impedance of the voltage supply source connected to the (VIN) input pins. If the impedance of this power supply were to increase, input voltage (VIN) could become unstable, leading to oscillation or lowered ripple rejection function. While a low-ESR $22\mu\text{F}$ capacitor with minimal susceptibility to temperature is recommended, stability is highly dependent on the input power supply characteristics and the substrate wiring pattern. In light of this information, please confirm operation across a variety of temperature and load conditions.   |
| C4        | $0.01\mu\text{F}$                                       | The Non Rush Current on Startup (NRCS) function is built into the IC to prevent rush current from going through the load (VIN to VO) and impacting output capacitors at power supply start-up. Constant current comes from the NRCS pin when EN is HIGH or the UVLO function is deactivated. The temporary reference voltage is proportionate to time, due to the current charge of the NRCS pin capacitor, and output voltage start-up is proportionate to this reference voltage. Capacitors with low susceptibility to temperature are recommended, in order to assure a stable soft-start time.   |
| C5        | -   | This component is employed when the C3 capacitor causes, or may cause, oscillation. It provides more precise internal phase correction.   |
| R5        | $100\text{k}$   | It is pull-up resistance of Open Drain pin. $100\text{k}\Omega$ is recommended.   |
| R4        | Several $\text{k}\Omega$<br>~several $10\text{k}\Omega$ | It is recommended that a resistance (several $\text{k}\Omega$ to several $10\text{k}\Omega$ ) be put in R4, in case negative voltage is applied in EN pin.  |

## ● Input-Output Equivalent Circuit Diagram



## ● Reference landing pattern



(Unit : mm)

| Lead pitch         | Lead pitch        | landing length | landing pitch |
|--------------------|-------------------|----------------|---------------|
| e                  | MIE               | $\geq 12$      | b2            |
| 0.65               | 2.50              | 0.40           | 0.35          |
| central pad length | central pad pitch |                |               |
| D3                 | E3                |                |               |
| 3.00               | 1.90              |                |               |

\*It is recommended to design suitable for the actual application.

# ●Notes for Use

## 1. Absolute maximum ratings

An excess in the absolute maximum ratings, such as supply voltage, temperature range of operating conditions, etc., can break down the devices, thus making impossible to identify breaking mode, such as a short circuit or an open circuit. If any over rated values will expect to exceed the absolute maximum ratings, consider adding circuit protection devices, such as fuses.

## 2. GND voltage

The potential of GND pin must be minimum potential in all operating conditions.

## 3. Thermal design

Use a thermal design that allows for a sufficient margin in light of the power dissipation (Pd) in actual operating conditions.

## 4. Actions in strong electromagnetic field

Use caution when using the IC in the presence of a strong electromagnetic field as doing so may cause the IC to malfunction.

## 5. ASO

When using the IC, set the output transistor so that it does not exceed absolute maximum ratings or ASO.

## 6. Thermal shutdown circuit

The IC incorporates a built-in thermal shutdown circuit (TSD circuit: Latch type). The thermal shutdown circuit (TSD circuit: Latch type) is designed only to shut the IC off to prevent thermal runaway. It is not designed to protect the IC or guarantee its operation.

Do not continue to use the IC after operating this circuit or use the IC in an environment where the operation of this circuit is assumed.

| TSD ON temperature<br>[°C] (typ.) | Hysteresis temperature [°C]<br>(typ.) |
|-----------------------------------|---------------------------------------|
| 175                               | 15                                    |

## 7. Ground Wiring Pattern

When using both small signal and large current GND patterns, it is recommended to isolate the two ground patterns, placing a single ground point at the ground potential of application so that the pattern wiring resistance and voltage variations caused by large currents do not cause variations in the small signal ground voltage. Be careful not to change the GND wiring pattern of any external components, either.

## 8. Output voltage resistance setting (R1, R2)

Output voltage resistance is adjusted with resistor R1 and R2. This IC is calculated as  $V_{FB} \times (R1+R2) / R1$ . Total 10kΩ is recommended so that the output voltage is not affected by the  $V_{FB}$  bias current.

## 9. Output capacitors (C3)

To assure output voltage stability, please be certain the  $V_{O1}$ ,  $V_{O2}$ , and  $V_{O3}$  pins and the GND pins are connected. Output capacitors play a role in loop gain phase compensation and in mitigating output fluctuation during rapid changes in load level. Insufficient capacitance may cause oscillation, while high equivalent series resistance (ESR) will exacerbate output voltage fluctuation under rapid load change conditions. While a 47μF ceramic capacitor is recommended, actual stability is highly dependent on temperature and load conditions. Also, note that connecting different types of capacitors in series may result in insufficient total phase compensation, thus causing oscillation. In light of this information, please confirm operation across a variety of temperature and load conditions.

## 10. Input capacitors setting (C1, C2)

Input capacitors reduce the impedance of the voltage supply source connected to the (VCC, VIN) input pins. If the impedance of this power supply were to increase, input voltage (VCC, VIN) could become unstable, leading to oscillation or lowered ripple rejection function. Stability highly depends on the input power supply characteristic and the substrate wiring pattern. Please confirm operation across a variety of temperature and load conditions.

**11. NRCS pin capacitors setting (Cnracs)**

The Non Rush Current on Startup (NRCS) function is built in the IC to prevent rush current from going through the load (VIN to VO) and impacting output capacitors at power supply start-up. The constant current comes from the NRCS pin when EN is HIGH or the UVLO function is deactivated. The temporary reference voltage is proportionate to time, due to the current charge of the NRCS pin capacitor, and output voltage start-up is proportionate to this reference voltage. To obtain a stable NRCS delay time, capacitors with low susceptibility to temperature are recommended.

**12. Input pins (Vcc, VIN, EN)**

This IC's EN pin, VIN pin, and VCC pin are isolated, and the UVLO function is built in the VCC pin to prevent undervoltage lockout. It does not depend on the Input pin order. Output voltage starts up when VCC and EN reach the threshold voltage. However, note that when putting in VIN pin lastly, VO may result in overshooting.

**13. Heat sink (FIN)**

Since the heat sink (FIN) is connected to with the Sub, short it to the GND. It is possible to minimize the thermal resistance by soldering it to substrate. Please solder properly.

**14. Please add a protection diode when a large inductance component is connected to the output terminal, and reverse-polarity power is possible at start-up or in output OFF condition.****15. Short-circuits between pins and mounting errors**

Please be sure to install the IC in correct position and orientation. Mounting errors, such as incorrect positioning or orientation, or connecting of the power supply in reverse polarity can also destroy the IC. Short-circuit between pins or pin and the power supply, or between ground may also damage to the IC.

## ●Heat Loss

Thermal design should allow operation within the following conditions. Note that the temperatures listed are the allowed temperature limits, and thermal design should allow sufficient margin from the limits.

1. Ambient temperature  $T_a$  can be no higher than 100°C.
2. Chip junction temperature ( $T_j$ ) can be no higher than 150°C.

Chip junction temperature can be determined as follows:

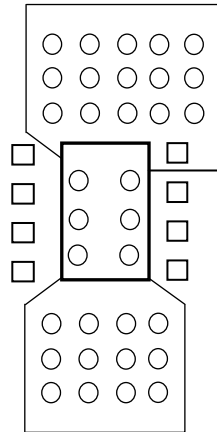
- ① Calculation based on ambient temperature ( $T_a$ )

$$T_j = T_a + \theta_{j-a} \times W$$

<Reference values>

|                              |   |  |
|------------------------------|---|--|
| $\theta_{j-a}$ :VSON010V3030 | 178.6°C/W   | 1-layer substrate (copper foil density 0.2%) |
|                              | 98.4°C/W  | 1-layer substrate (copper foil density 7%)   |
|                              | 41.3°C/W  | 2-layer substrate (copper foil density 65%)  |
|                              | Substrate size: 70 × 70 × 1.6mm <sup>3</sup> (substrate with thermal via) |  |

It is recommended to layout the VIA for heat radiation in the GND pattern of reverse (of IC) when there is the GND pattern in the inner layer (in using multiplayer substrate). This package is so small (size: 3.0mm × 3.0mm) that it is not available to layout the VIA in the bottom of IC. Spreading the pattern and being increased the number of VIA like the figure below). enable to get the superior heat radiation characteristic. (This figure is the image. It is recommended that the VIA size and the number is designed suitable for the actual situation.).



Most of the heat loss that occurs in the BD354XNUV is generated from the output Nch FET. Power loss is determined by the total  $V_{IN}$ - $V_o$  voltage and output current. Be sure to confirm the system input and output voltage and the output current conditions in relation to the heat dissipation characteristics of the  $V_{IN}$  and  $V_o$  in the design. Bearing in mind that heat dissipation may vary substantially depending on the substrate employed (due to the power package incorporated in the BD354XNUV) make certain to factor conditions such as substrate size into the thermal design.

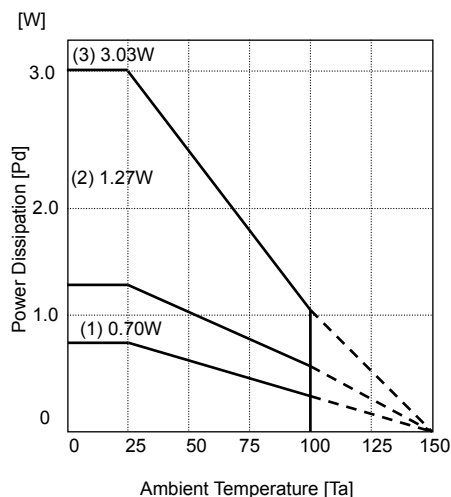
$$\text{Power consumption (W)} = \left\{ \text{Input voltage (V}_{IN}\text{)} - \text{Output voltage (V}_o\text{)} \left( V_o \doteq V_{REF} \right) \right\} \times I_o(Ave)$$

Example) Where  $V_{IN}=1.7V$ ,  $V_o=1.2V$ ,  $I_o(Ave) = 1A$ ,

$$\begin{aligned} \text{Power consumption (W)} &= \left\{ 1.7(V) - 1.2(V) \right\} \times 1.0(A) \\ &= 0.5(W) \end{aligned}$$

## ●Heat Dissipation Characteristics

VSON010V3030



- (1) Substrate (copper foil density: 0.2%...1-layer)  
 $\theta_{j-a}=178.6^\circ\text{C/W}$
- (2) Substrate (copper foil density: 7%...1-layer)  
 $\theta_{j-a}=98.4^\circ\text{C/W}$
- (3) Substrate (copper foil density: 65%...1-layer)  
 $\theta_{j-a}=41.3^\circ\text{C/W}$

●Ordering part number

|   |   |
|---|---|
| B | D |
|---|---|

Part No.

|   |   |   |   |
|---|---|---|---|
| 3 | 5 | 4 | 0 |
|---|---|---|---|

Part No.  
3540 , 3541

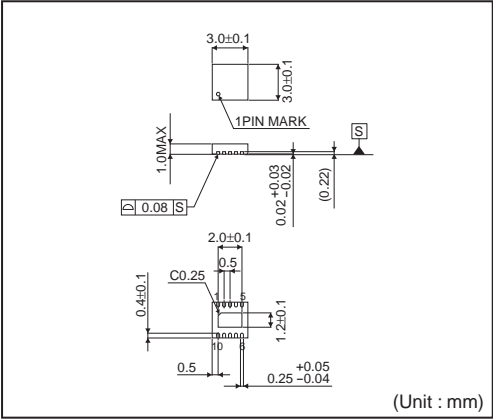
|   |   |   |
|---|---|---|
| N | U | V |
|---|---|---|

Package  
NUV : VSON010V3030

|   |   |
|---|---|
| E | 2 |
|---|---|

Packaging and forming specification  
E2: Embossed tape and reel

VSON010V3030



<Tape and Reel information>

|                   |  |
|-------------------|--|
| Tape              | Embossed carrier tape  |
| Quantity          | 3000pcs  |
| Direction of feed | E2<br>( The direction is the 1 pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand ) |

Reel

1 pin

Direction of feed

\*Order quantity needs to be multiple of the minimum quantity.



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